Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Claims 1-12 (Canceled).

13. (Previously Presented) In a memory redundancy circuit in a memory module having a designated group of memory cells assigned to represent a logical portion of the memory structure and a redundant group of memory cells, the method comprising assigning the redundant group to the logical portion of the memory structure, responsive to a preselected designated group condition.

14. (Previously Presented) The method of Claim 13, wherein the assigning comprises shifting data to the redundant group of memory cells responsive to a signal representative of the preselected designated group condition.

15. (Previously Presented) The method of Claim 13, wherein the memory module further comprises a plurality of selectable switches, the plurality of selectable switches encoding the preselected designated group condition.

16. (Previously Presented) The method of Claim 15, wherein the plurality of selectable switches comprises fuses.

17. (Previously Presented) The method of Claim 15, wherein the preselected designated group condition comprises a "FAILED" condition, representative of a designated malfunction.

18. (Previously Presented) The method of Claim 13, wherein each of the designated group of memory cells and the redundant group of memory cells comprises one of a memory row, a memory column, a preselected portion of a memory module, a selectable portion of a memory module, a memory module, and a combination thereof.

Claims 19-24 (Cancelled)

25. (Previously Presented) In a memory circuit including designated memory cells, redundant memory cells and a controller, a method comprising redirecting a signal path from the designated memory cells to the redundant memory cells based on a failure of at least a portion of the designated memory cells, the controller comprising a plurality of selectable switches having a logarithmic relationship to the number of designated memory cells.

26. (Previously Presented) The method of claim 25 wherein the redirecting comprises shifting data to at least a portion of the redundant group of memory cells responsive to a signal representative of the failure of at least a portion of the designated memory cells.

27. (Previously Presented) The method of Claim 25, wherein the plurality of selectable switches comprises fuses.

28. (Previously Presented) The method of Claim 25, wherein the designated memory cells and the redundant memory cells each comprises one of a row pair of memory cells and a column pair of memory cells.

29. (Previously Presented) The method of Claim 25, wherein the designated memory cells and the redundant memory cells each comprises a line pair of memory cells.

30. (New) In a memory circuit, a method comprising redirecting a signal path from designated memory cells to redundant memory cells based on a failure of the designated memory cells, wherein the redirecting comprises shifting data to at least a portion of the redundant memory cells responsive to a signal representative of a preselected designated condition of at least a portion of the designated memory cells.

31. (New) The method of claim 30, wherein the designated memory cells comprise pairs of designated memory cells.

32. (New) The method of claim 31,

wherein the memory circuit comprises a plurality of selectable switches, and

wherein the plurality of selectable switches encode an encoded signal and have a logarithmic relationship to the number of pairs of designated memory cells.

33. (New) The method of claim 32, wherein the plurality of selectable switches comprise fuses.

34. (New) The method of claim 30, wherein the designated memory cells or the redundant memory cells comprise row pairs of memory cells

35. (New) The method of claim 30, wherein the designated memory cells or the redundant memory cells comprise column pairs of memory cells.

36. (New) The method of claim 30, wherein the designated memory cells and the redundant memory cell comprise line pairs of memory cells.

37. (New) The method of claim 30, wherein the redundant memory cells are pairs of redundant memory cells.

38. (New) The method of claim 37, wherein the designated memory cells are pairs of designated memory cells.

39. (New) The method of claim 30, wherein the redundant memory cells comprise pairs of redundant memory cells.